CLAIMS

What is claimed is:

1. A dense memory cell comprising:

two access transistors, each having a gate tied to a wordline input, a first one of the access transistors having a drain and source coupled between a bit line and an output node;

two storage transistors, a first one having a drain and source coupled between the output line and a power signal and a gate couple to an output bar node, the second one having a drain and source coupled between the output bar node and the power rail, and a gate coupled to the output node; and

a control circuit generating a tracking voltage coupled to the wordline, the track voltage for adjusting the voltage on the wordline during an idle state to ensure that leakage current through the two access transistors exceeds the leakage through the two storage transistors where the output node to which it is coupled is at VDD.

2. The memory cell of Claim 1 wherein the tracking voltage is a function of a reference voltage determined to provide a leakage through the access transistors that exceeds the leakage through the storage devices.

3. The memory cell of Claim 2 wherein the tracking voltage is maintained substantially constant by a differential amplifier.

4. The memory cell of Claim 3 wherein the tracking voltage is buffered to substantially reduce disturbances to VREF resulting from switching states on the wordline.

5. The memory cell of Claim 3 wherein the tracking voltage is generated by a reference circuit, the reference circuit comprising:

a plurality of partial memory cells, each partial memory cell comprising one access transistor and storage transistor configured in a worst case leakage condition; and

a differential amplifier having a voltage reference input and a second input coupled to an output node of each of the partial memory cells, the output of the differential amplifier being the tracking voltage.

6. The memory cell of Claim 1 wherein the tracking voltage is coupled to an N-well comprising storage transistors.

7. The memory cell of Claim 1 wherein the tracking voltage is coupled to the V_{ss} connection to which the storage transistors are coupled.

8. A method of maintaining a preferred leakage ratio between access and storage devices in a memory cell, said method comprising:

establishing a reference voltage that is equal to a desired output voltage of the cell;

generating a tracking signal required to force the reference voltage onto an output of a dummy circuit; and

coupling the tracking signal to a point in the memory cell whereby the leakage ratio is favorably maintained.

9. A dense memory cell comprising:

two access transistors, each having a gate tied to a well bias input, a first one of the access transistors having a drain and source coupled between a bit line and an output node;

two storage transistors, a first one having a drain and source coupled between the output line and a power signal and a gate couple to an output bar node, the second one having a drain and source coupled between the output bar node and the power signal, and a gate coupled to the output node; and

a control circuit generating a tracking voltage coupled to the well bias, the track voltage for adjusting the voltage on the well bias during an idle state to ensure that leakage current through the two access transistors exceeds the leakage through the two storage transistors where the output node to which it is coupled is at VDD.

10. The memory cell of Claim 9 wherein the track voltage is a function of a reference voltage determined to provide a leakage through the storage transistors that is less than the leakage through the access devices.

11. A dense memory cell comprising:

two access transistors, each having a gate tied to a power signal input, a first one of the access transistors having a drain and source coupled between a bit line and an output node;

two storage transistors, a first one having a drain and source coupled between the output line and the power signal and a gate couple to an output bar node, the second one having a drain and source coupled between the output bar node and the power rail, and a gate coupled to the output node; and

a control circuit generating a tracking voltage coupled to the power signal, the track voltage for adjusting the voltage on the power signal during an idle state to ensure that leakage current through the two access transistors exceeds the leakage through the two storage transistors where the output node to which it is coupled is at VDD.

12. The memory cell of Claim 10 wherein the track voltage is a function of a reference voltage determined to provide a leakage through the storage transistors that is less than the leakage through the access devices.